WHAT IS CLAIMED IS:

1. A contactless mask programmable read-only memory (Mask ROM), comprising a plurality of MOS-type memory cells, wherein

the memory cells include a plurality of first memory cells and a plurality of second memory cells, wherein the first memory cells have a first channel conductivity and are depletion MOS transistors, and the second memory cells have a second channel conductivity and are enhanced MOS transistors; and

a memory cell shares two diffusions with two adjacent memory cells that are aligned with the memory cell along a first direction.

2. The contactless Mask ROM of claim 1, wherein the memory cells comprise NMOS transistors, the first memory cells comprise depletion NMOS transistors that have N-type channels, and the second memory cells comprise enhanced NMOS transistors that have P-type channels.

3. The contactless Mask ROM of claim 1, wherein the N-type channels of the depletion NMOS transistors are doped with phosphorous (P) or arsenic (As).

4. The contactless Mask ROM of claim 1, wherein the memory cells comprise PMOS transistors, the first memory cells comprise depletion PMOS transistors that have P-type channels, and the second memory cells comprise enhanced PMOS transistors that have N-type channels.

5. The contactless Mask ROM of claim 1, further comprising a plurality of word lines oriented in a second direction different form the first direction, wherein

gate electrodes of a first string of memory cells that are arranged along the second direction are coupled to a word line; and

a diffusion of one terminal memory cell in a second string of memory cells

that are arranged along the first direction is coupled to a first voltage source of a first level, and a diffusion of the other terminal memory cell in the second string of memory cells is coupled to a second voltage source of a second level, wherein the first level is different from the second level.

6. The contactless Mask ROM of claim 5, wherein the gate electrodes of the first string of memory cells themselves are formed as a word line.

7. The contactless Mask ROM of claim 5, further comprising a plurality of bit lines oriented in the first direction, wherein a bit line serves as the first voltage source.

8. The contactless Mask ROM of claim 5, wherein the second voltage source comprises a ground voltage source.

9. The contactless Mask ROM of claim 5, wherein the word lines comprise doped polysilicon.

10. The contactless Mask ROM of claim 1, wherein two adjacent strings of memory cells that are oriented in the first direction are separated by an isolation layer.

11. A contactless Mask ROM, comprising:

a plurality of word lines extending along a row direction; and

a plurality of MOS-type memory cells arranged in rows and columns, including a plurality of first memory cells that have a first channel conductivity and are depletion MOS transistors, and a plurality of second memory cells that have a second channel conductivity and are enhanced MOS transistors, wherein

a word line is constituted by gate electrodes of the memory cells in one row;

a memory cell shares two diffusions with two adjacent memory cells in the

same column; and

a diffusion of one terminal memory cell in a column of memory cells is coupled to a first voltage source of a first level, and a diffusion of the other terminal memory cell is coupled to a second voltage source of a second level, wherein the first level is different from the second level.

12. The contactless Mask ROM of claim 11, wherein the memory cells comprise NMOS transistors, the first memory cells comprise depletion NMOS transistors that have N-type channels, and the second memory cells comprise enhanced NMOS transistors that have P-type channels.

13. The contactless Mask ROM of claim 11, wherein the memory cells comprise PMOS transistors, the first memory cells comprise depletion PMOS transistors that have P-type channels, and the second memory cells comprise enhanced PMOS transistors that have N-type channels.

14. The contactless Mask ROM of claim 11, further comprising a plurality of bit lines, wherein a bit line serves as the first voltage source.

15. The contactless Mask ROM of claim 11, wherein the second voltage source comprises a ground voltage source.

16. The contactless Mask ROM of claim 11, wherein two adjacent columns of memory cells are separated by an isolation layer.

17. A NAND Mask ROM, comprising a plurality of word lines, a plurality of bit lines, and a plurality of memory cells arranged in rows and columns, wherein

the memory cells include a plurality of first memory cells that have a first channel conductivity and are depletion MOS transistors, and a plurality of second memory cells that have a second channel conductivity and are enhanced MOS

transistors;

the memory cells in the same row are coupled to a word line, and the memory cells in the same column are coupled to a bit line;

a constant number of continuous memory cells in the same column are grouped as a memory string, wherein

a non-terminal memory cell shares a source and a drain with two adjacent memory cells in the memory string; and

one terminal memory cell in the memory string is coupled to a bit line, and the other terminal memory cell is coupled to ground.

18. The NAND Mask ROM of claim 17, wherein the memory cells comprise NMOS transistors, the first memory cells comprise depletion NMOS transistors that have N-type channels, and the second memory cells comprise enhanced NMOS transistors that have P-type channels.

19. The NAND Mask ROM of claim 17, wherein the memory cells comprise PMOS transistors, the first memory cells comprise depletion PMOS transistors that have P-type channels, and the second memory cells comprise enhanced PMOS transistors that have N-type channels.

20. The NAND Mask ROM of claim 17, wherein gate electrodes of the memory cells in the same row are coupled to a word line with contacts.

21. The NAND Mask ROM of claim 17, wherein two memory strings adjacent in the row direction share one bit line, the two adjacent memory strings consisting of a first memory string and a second memory string.

22. The NAND Mask ROM of claim 21, wherein

each memory string is selected with a pair of bank select transistors,

including a depletion MOS transistor and an enhanced MOS transistor that are coupled, wherein one of the two bank select transistors is coupled to a terminal memory cell in the memory string;

the two pairs of bank select transistors of the are arranged in two rows and two columns, wherein two bank select transistors in the same row are coupled to a bank select line with gate electrodes thereof, and two terminal bank select transistors accompanied with the two adjacent memory strings are coupled to the bit line; and

the depletion (or enhanced) MOS transistor among the pair of bank select transistors for selecting the first memory string is coupled to a bank select line together with the enhanced (or depletion) MOS transistor among the pair of bank select transistors for selecting the second memory string.

23. The NAND Mask ROM of claim 22, wherein one of the two bank select transistors for selecting a memory string shares a diffusion with a terminal memory cell in the memory string.

24. The NAND Mask ROM of claim 22, wherein the depletion MOS transistor and the enhanced MOS transistor in a pair of bank select transistors for selecting a memory string share a diffusion.

25. The NAND Mask ROM of claim 22, wherein the two terminal bank select transistors accompanied with the two adjacent memory strings share a diffusion that is coupled to the bit line.

26. The NAND Mask ROM of claim 17, wherein a memory string is coupled to a bit line, and does not share the bit line with another memory string adjacent in the row direction.

27. The NAND Mask ROM of claim 26, wherein one terminal memory cell in a memory string is coupled to a bit line via one bank select transistor.

28. The NAND Mask ROM of claim 17, wherein a diffusion of the other terminal memory cell in the memory string is coupled to a ground line via a contact.

29. The NAND Mask ROM of claim 17, wherein two memory strings are separated by an isolation layer.

30. The NAND Mask ROM of claim 17, wherein the constant number is 8.